

A METHOD AND SYSTEM FOR CODING TEST
PATTERN FOR SCAN DESIGN

ABSTRACT OF THE DISCLOSURE:

A method and system for efficiently coding test pattern for ICs
5 in scan design and build-in linear feedback shift register (LFSR)
for pseudo-random pattern generation. In an initialization
procedure, a novel LFSR logic model is generated and integrated
into the system for test data generation and test vector
compression. In a test data generation procedure, test vectors
10 are specified and compressed using the LFSR logic model. Every
single one of the test vectors is compressed independently from
the others. The result, however, may be presented all at once and
subsequently provided to the user or another system for further
processing or implementing in an integrated circuit to be tested.
15 According to the present invention a test vector containing
0/1-values for, e.g., up to 500.000 shift registers and having,
e.g., about 50 so called care-bits can be compressed to a compact
pattern code of the number of care-bits, i.e., 50 bits for the
example of 50 care-bits.